REMARKS

Reconsideration of the above identified application in view of the preceding amendments and following remarks is respectfully requested.

Claims 13, 17, 34 and 35 are pending in this application. By this Amendment, Applicants have amended Claims 13 and 34. New Claim 35 has been added by this amendment. The claim amendments were made to more precisely define the invention in accordance with 35 U.S.C. 112, paragraph 2. These amendments have not been necessitated by the need to distinguish the present invention from any prior art. It is respectfully submitted that no new matter has been introduced by these amendments, as support therefore is found throughout the specification and drawings.

In the Office Action, Claims 13 and 34 were rejected under 35 U.S.C. § 103 (a) over Takahashi in view of U.S. Patent No. 4,830,976 to Morris et al.

Takahashi et al. disclose a MOSFET having a polycide gate structure in which a polycrystalline silicon film, a dielectric film and another polycrystalline silicon film are consecutively deposited (see Abstract). To form the MOSFET with a lightly doped drain structure, side wall spacers 8 are formed (see col. 9, lines 1-14 and Figure 11). The side wall spacers 8 surround the polycrystalline silicon layer 2 and the dielectric film 1 thereon. The side wall spacers 8 are also rounded to provide the desired spacing effect.

Morris et al. disclose an integrated circuit with a resistor that is formed by doping a semiconductor region that is defined by a polysilicon layer that also defines the gate electrode of field effect transistors in the integrated circuit.

There is nothing in either of these references that discloses or suggests, either alone or in combination, in whole or in part, the device defined by Claim 13 of the subject application. In particular, there is nothing which discloses or suggests, a semiconductor device including a semiconductor layer substantially defining a plane, an MOS transistor formed on the semiconductor layer, a resistive conductive layer formed on the semiconductor layer, said

resistive conductive layer having a top surface opposing the semiconductor layer with a sidewall extending therebetween, a center part and two ends, a protective layer selected from the group consisting of a silicon nitride layer or a silicon oxynitride layer, the protective layer being formed on the top surface of the resistive conductive layer, and a silicon oxide insulating layer formed on the sidewall of the resistive conductive layer, the sidewall being substantially planar, perpendicular to the plane and underneath the protective layer, wherein widths of said two ends of said resistive conductive layers are wider than a width of said center part of said resistive conductive layer. Consequently, the silicon oxide insulating layer is a relatively straight sidewall underneath the protective layer. The spacers 8 of Takahashi et al. are rounded and extend up to the top of the dielectric film 1. Thus, Takahashi et al. do not disclose the claimed structure and Morris et al. do not cure this deficiency. In view of this, Claim 13 of the subject application is not rendered obvious by the combination of references cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

Turning to Claim 34, it recites a semiconductor device including a semiconductor layer, an MOS transistor formed on the semiconductor layer, a resistive conductive layer formed on the semiconductor layer, said resistive conductive layer having a substantially vertical sidewall, a center part and two ends, a protective layer formed on the resistive conductive layer and an insulating layer formed on the sidewall of the resistive layer, the insulating layer having a substantially vertical outer sidewall, wherein widths of said two ends of said resistive conductive layer are wider than a width of said center part of said resistive conductive layer. The spacers 8 of Takahashi et al. are rounded. Morris et al. do not cure this deficiency. Thus, the cited combination does not disclose the claimed structure of the substantially vertical sidewall of the insulating layer. In view of this, Claim 34 of the subject application is also not rendered obvious by the combination of references cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

In the Office Action, Claim 17 was rejected under 35 U.S.C. § 103 (a) over Takahashi in view of U.S. Patent No. 4,830,976 to Morris et al. and further in view of U.S. Patent Publication No. 2003/0034531 to Kanda et al. Claim 17 depends from Claim 13 thus the arguments noted above are equally as applicable hereto. Thus, for at least the same reasons, Claim 17 is also not rendered obvious by the combination of references cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

Applicant has added new Claim 35, which depends from Claim 13 and is allowable for the same reasons as noted above. Among other places, support for Claim 34 can be found at page 17, first three paragraphs of the subject application.

In view of the above amendment, applicant believes the pending application is in condition for allowance, and such action is earnestly solicited.

Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105. If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

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Respectfully submitted,

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